Microwave Review
July 2024, Vol. 30, No. 1, pp. 55-66
DOI: 10.18485/mtts_mr.2024.30.1.8

2.4 GHz low noise amplifier: A comprehensive review and pioneering research contributions for RF applications

T. Snehitha Reddy, Vijay Nath

Abstract – **This paper presents an overview of the different types of low noise amplifiers (LNAs) at 2.4 GHz frequency and the design of a single-stage inductive degenerated common-source narrow-band low-noise amplifier with a current reuse technique. The CLC with current reuse at the source forms an input-matching configuration in the common source input stage. Because of the CLC circuit used, the LNA achieved impedance matching between the source and the input of the LNA. The current reuse technique used here ensured an enhanced gain. The low noise amplifier simulated in Cadence Virtuoso 180 nm library achieved a gain of 23.06 dB with a noise figure of 0.15 dB. The S_{11} is -17.17 dB, S_{22} is -16.4 dB and S_{12} is at -45.5 dB. The power consumed is 5 mW and has unconditional stability with a stability factor k_f of 6.8. Corner analyses validate the stability of the circuit despite variations in process, voltage, and temperature (PVT). The layout of the circuit leaves a footprint of 1.2mm x0.83mm.**

Keywords - **Common source (CS), Inductive source degeneration (ISD), Microstrip lines, Noise figure (NF), S- parameters, Third order input intercept point (IIP_3).**

I. INTRODUCTION

Technological advancements in complementary metal-oxide-semiconductors (CMOS) have made communication systems more accessible, and these advancements are increasingly incorporated into radio frequency (RF) designs [1-5]. RF waves have a frequency range from 3 kHz to 300 GHz and are used in various electronics and devices, such as television broadcasting, cellular telephones, and satellite communications. In wireless communication, an RF signal is a wireless electromagnetic signal transmitted between a transmitter and a receiver. Various applications for wireless communication use different frequencies, including IRNSS, radar, Wi-Fi, Bluetooth, and Wireless Local Area Network (WLAN) [6, 7].

For various applications of Low noise amplifiers (LNAs), several circuits with different configurations have been suggested [8,9]. Common source low noise amplifier (CS-LNA) provides exceptional noise reduction and gain enhancement performance. The addition of an inductor to the source of a common source (CS) stage creates the widely recognized Induction Source Degeneration (ISD) effect, which affects the gain and noise performance of the LNA [10].

Article history: Received November 9, 2023; Accepted December, 11,2023

Reddy T.S, and Nath V, are with Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India, 835215. E-mail: phdec10004.21@bitmesra.ac.in, vijaynath@bitmesra.ac.in

Common gate (CG) configuration in common gate low noise amplifier (CG-LNA) yields a stable, low-power circuit that is less susceptible to parasitic interference. To improve the noise performance of the CG stage, various techniques, such as capacitive cross-coupling, can be employed [11]. Although the conventional common-gate low-noise amplifier (CG-LNA) offers better linearity, input matching, and stability compared to inductively degenerated common-source LNAs, due to its relatively high noise figure (NF) at low working frequencies, it has not been used extensively [12-17].

The source follower topology does not require a drain resistor since the terminal is connected to the ground. On the other hand, the common drain topology exhibits low output impedance and high input impedance. Each LNA configuration and topology has its advantages and disadvantages, and the appropriate choice depends on the specific application requirements.

This paper presents an analysis and comparison of low-noise amplifiers operating at 2.4 GHz. The LNAs are designed using various tools such as Cadence and ADS software, different topologies including common source and inductive degeneration, and components such as passive RLC, microstrip lines, and stubs.

This research primarily focuses on the development of a narrow-band (NB) Low-Noise Amplifier (LNA) with the key objective of achieving a low noise figure and high gain, addressing a limitation observed in prior studies where noise figures exceeded 2 dB. After evaluating the performance of the previous LNAs mentioned in Section 2, we proceeded to design a novel circuit using Cadence Virtuoso. The resulting circuit demonstrated superior performance in terms of gain, noise figure, and overall stability. The reduction in noise figure, along with increased gain, can be mainly attributed to the incorporation of the current reuse technique, interstage CLC circuit, and optimized impedance matching networks. This combination of techniques not only improves the input impedance but also effectively reduces noise at the input stage.

Section 2 briefly describes the works of different articles with different applications. Section 3 discusses the proposed LNA. Section 4 concludes the summary of the said review article. Table 1 summarizes the comparison of different LNAs.

II. LITERATURE REVIEW

A. D. Jahnavi's low-noise amplifier [7]

To determine the best topology for the task, the author examined four potential single-stage cascode configurations: shunt-resistive feedback cascode, common source (CS)

cascode, current reuse cascode, and common gate (CG) cascode. Each topology was designed and evaluated based on its performance parameters, including noise figure (NF), gain, stability, and return losses. Notably, each topology has its own limitations. The author's focus was on developing a single-stage, single-band LNA for IRNSS applications in the S-band, with a centre frequency of 2.492 GHz, that would have the lowest possible noise figure and highest possible gain.

The designed circuit in Fig. 1 incorporates a common source (CS) cascode configuration with current reuse and an interstage series LC circuit to achieve a high gain and low noise figure.

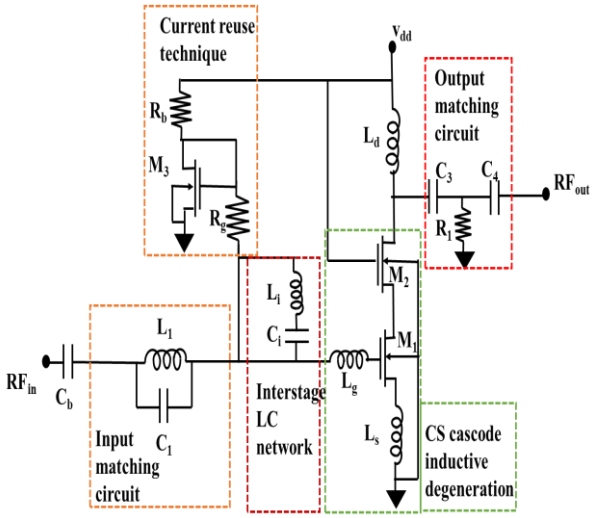

Fig. 1. Common Source (CS) LNA [7]

The noise analysis in this study considers two primary noise sources: resistors and transistors. The noise source resulting from resistors is determined using Eq. (1):

$$e_n^2 = 4KT\delta R\Delta f \tag{1}$$

and MOS device's noise is given in Eq. (2):

$$i_n^2 = 4KT\gamma g_m \Delta f \tag{2}$$

where K is Boltzmann's constant, γ and δ are defined as the noise parameters of the MOSFET and resistor respectively, Δf is Bandwidth and gm is the transconductance.

According to the author, the addition of tuned LC components at the input end has achieved narrowband matching, which is particularly useful for frequencies ranging from 30 to 300 MHz.

The proposed circuit diagram (Fig 1.) provides a clear representation of the various techniques used, making it easily understandable for readers. Although the author was able to improve gain and minimize noise, better input-output matching was not achieved despite the addition of extra-tuned LC components.

B. I.E Yilmaz's low noise amplifier (LNA) [18]

The author has utilized microstrip transmission lines to create circuit components for low-noise amplifiers, including transistor schematics and input-output matching circuits. FR4 is the chosen substrate surface due to its affordability and accessibility. To amplify the signal, a two-stage circuit is employed while a series feedback technique is utilized to decrease the noise figure. The input-output matching networks incorporate transmission lines that use pi matching with open circuit termination. This ensures proper connection between the ports and transmission lines.

Instead of the commonly used Cadence Spectre RF for design and analysis, the design utilizes the optimized tool of Cadence, namely the Cadence AWR DE (Design Environment) MWO (Microwave Office) program. The AWR MWO optimizer tool is used to adjust the width and length of transmission lines in the design.

The block diagram illustrating the fundamental concept of this low-noise amplifier is presented in Fig. 2. The diagram exhibits a sequential arrangement of the input matching network, transistor circuit, and output matching network, along with a DC supply utilized for transistor biasing

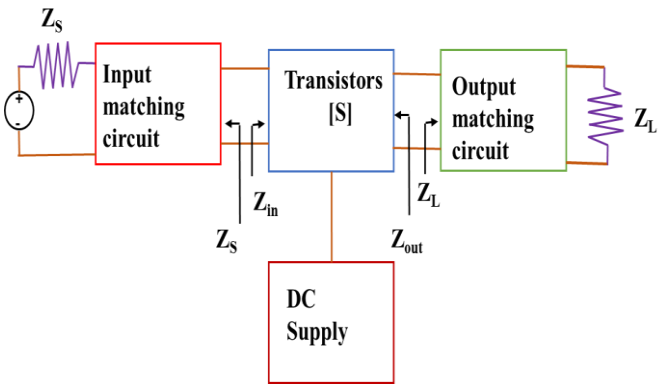

Fig. 2. Block diagram of the basic concept of LNA [18]

The noise analysis is given by Eq. (3):

$$NF = 10(F) = 10\frac{SNR_i}{SNR_o} \tag{3}$$

where, NF is the noise figure, F is the noise factor, SNR_i is the input signal-to-noise ratio, SNR_o is the output signal-to-noise ratio.

The designed LNA aimed to achieve high gain and low noise with minimal power consumption. However, while the former objectives were met, there is no clear mention of the power consumption value. Although the utilization of microstrip transmission lines is innovative, the transistor configuration topology used in the design is not specified. The return losses of the LNA are promising, as they are less than -10dB. However, the lack of proper input-output matching is evident in the values of S_{11} and S_{22}, which are -10 dB and -19.07 dB, respectively, for this design.

C. S. A. Zainol Murad's low-noise amplifier [19]

The primary focus of the author was to achieve low power consumption in the LNA. To meet this objective, a two-stage ultralow power LNA was designed using the forward body bias technique. The two-stage configuration was chosen to increase the gain while simultaneously reducing power consumption. The minimum supply voltage in cascode configurations is usually 2 V_{th}, which is not appropriate for

low-power applications. However, the author has utilized the forward body bias technique to address this issue.

The designed LNA utilizes the forward body bias technique for low power consumption in both stages. Additionally, the current reuse technique is employed to decrease the supply voltage and current. However, the drawback of this reduction is the decrease in gain. There are several gain-boosting techniques available that can be utilized to enhance the gain but at the cost of high-power consumption. These techniques have been explored in previous works [20-23] and are subject to a trade-off between gain and power consumption [19].

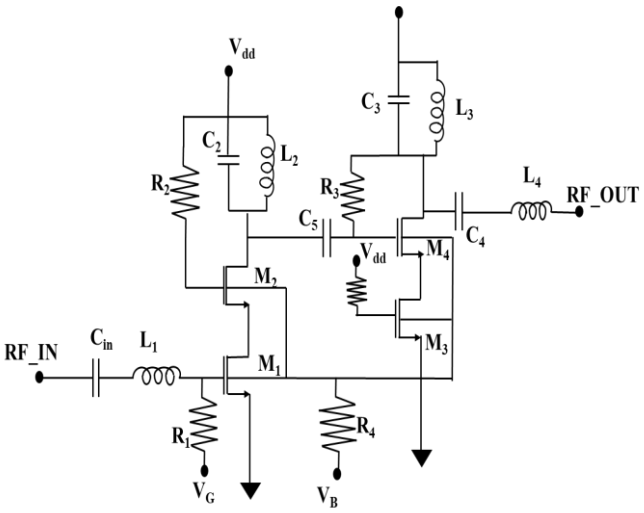

Fig. 3. Low noise amplifier for wireless applications [19]

The LNA design, as depicted in Fig. 3, comprises two transistors in a cascode configuration in each stage, and both stages are connected in a cascade structure. The total current drawn by the LNA is 1 mA, and it operates at a supply voltage of 0.55 V, consuming a total power of 0.55 mW. The width of the first-stage transistors is 130 µm, while the second-stage transistor width is 120 µm.

The input matching and gain improvement are primarily achieved with C_2 and L_2. Capacitors C_3 and C_4, along with inductors L_3 and L_4, are responsible for output matching, while capacitor C_5 takes care of interstage matching. The absence of a load resistor has helped reduce thermal noise.

The metric for evaluating the performance of the designed LNA is the figure of merit (FOM), which is computed as the ratio of power gain to power dissipation and the noise figure (NF) performance, as shown in Eq. (4):

$$FOM(mW^{(-1)}) = \frac{Gian_{abs}}{(NF-1)_{abs} \times P_{DC}} \qquad (4)$$

The author successfully achieved the goal of low power consumption by implementing a low power supply voltage, but other important parameters such as the input-output reflection coefficient, gain, and noise figure were not prioritized. In general, the reflection coefficient of any low noise amplifier should be less than -10 dB, but the achieved S_{11} and S_{22} values are positive and do not meet this requirement. The gain achieved is 12 dB, but the noise figure is 5.9 dB which is also not desirable. Therefore, there is room for improvement to increase the gain and reduce the noise figure.

D. R. Fiorelli's low-noise amplifier [24]

The single-ended inductive source degeneration topology is used to construct a common source LNA due to its advantages such as low cost and low power consumption. The amplification transistor M_1 depicted in Fig. 4 is biased in moderate inversion to restrict power consumption and enable the potential for reducing the supply voltage. The input impedance is achieved by adjusting inductors L_s and L_{g1}. An additional capacitor is added between the gate and source terminals of M_1 to decouple noise. To attain maximum gain, inductor L_d plays a crucial role. A control bit called CtrlG in the CS-LNA's input network allows you to choose between a high gain (hg) and a low gain (lg). By turning a current branch of the current-generating circuit on and off, this control modifies the ultimate bias current of the LNA. The source of the CS-current LNA includes a discrete gain control that allows for gain on two levels in this block. By selecting the low level, it is possible to avoid SW-MIX saturation when high-level input signals reach the front end.

In CMOS 90 nm technology with a 1.2 V voltage supply, the design of a differential switched transistor mixer and single-ended LNA as the receiver front-end have been completed. The area taken up by the LNA inductors, the external chip components, and the power consumption are all decreased by the single-ended input. The system achieves a minimum power consumption of 4.7 mW, and the lowest observed noise figure at 2.5 MHz of 7.5 dB.

E. B. Maruddani's low-noise amplifier [25]

In ADS software an LNA with a two-stage cascade using a microstrip line matching network with a single stub technique is designed. Antenna design validation is needed in simulations to determine the optimal performance of the LNA.

For the designed LNA shown in Fig. 5 the author has calculated stability using Eq. (5):

$$K = \frac{1 - |S_{11}|^2 - |S_{12}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \qquad (5)$$

$\Delta = S_{11}.S_{22} - S_{11}.S_{22}$ and here S_{11} is input reflection coefficient, S_{22} output reflection loss, S_{12} reverse transmission co-efficient, S_{21} gain. The author here has tabulated different values like S-parameters, noise figure, VSWR input, and VSWR output which are measured and simulated. There is an enormous difference in the measured values and simulated values in those mentioned parameters. Although there is good impedance matching there is no clear explanation as to how the input matching and output matching is attained. The gain achieved is approximately 30 dB and the noise figure is 1.248 dB which are excellent values. There were many equations for the calculation of different parameter values.

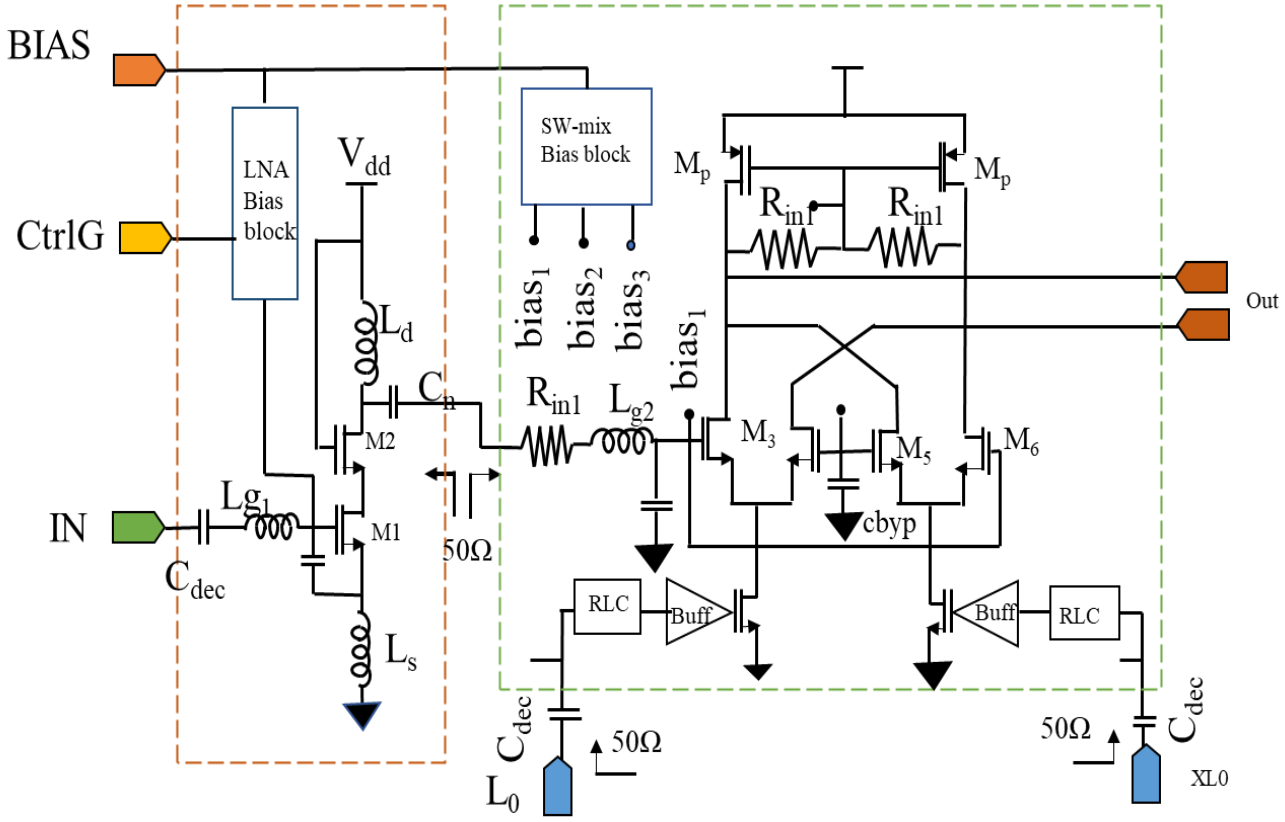

Fig. 4. LNA for ZigBee applications [24]

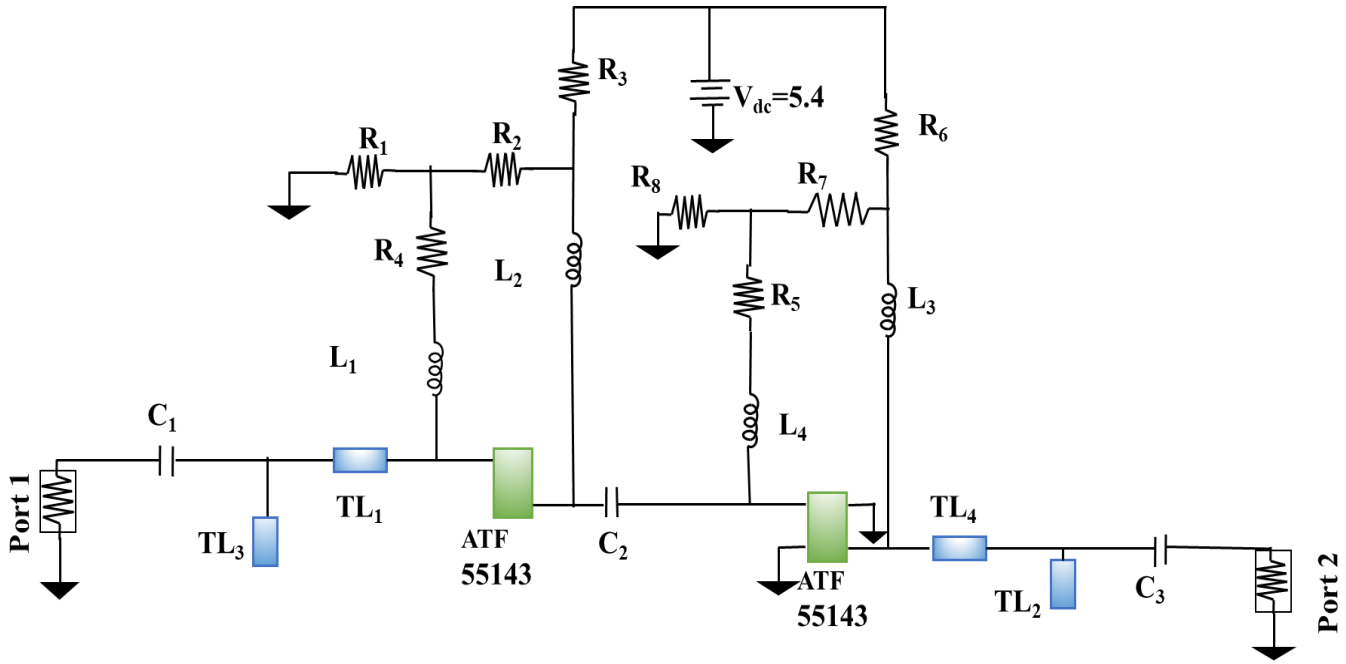

Fig. 5. Single-stage cascade LNA [25]

F. M. E. Bakkali's low-noise amplifier [26]

To design an LNA for wireless applications the author used an RF_4 substrate in planar technology. The selection of topology and transistors are two key important factors in RF design. The author here selected transistor ATF-21170 from Avago Technology which meets the required specifications. This transistor is a high electronic mobility transistor in enhancement mode.

A bias network with three ports is used for biasing here, where.

- Port (P_3) is a low frequency that is used to give the polarization,
- The radiofrequency signal is delivered by port (P_1), which is a high-frequency port, and
- A radiofrequency RF signal and DC are received by the third output port (P_2).

Without a series resistance at the transistor output, the stability factor (K_f) achieved was less than one, which shows the LNA is not unconditionally stable. To improve the stability of the amplifier, avoid self-oscillations, and properly function the amplifier, either a series or parallel resistor can be added to the load. To enhance the stability, the author appended a resistor in series to the transistor output. Fig. 6 shows a designed LNA for Wi-Fi applications. Three types of gains characterize the transistor which are transducer gain G_T, power gain G_P, and available gain G_A, which are dependent on S-parameters and are given by the following equations Eq. (6), (7) and (8):

$$G_T = \frac{P_L}{P_A} = \frac{|S_{21}|^2\left(1-|\Gamma_s|^2\right)\left(1-|\Gamma_L|^2\right)}{|1-S_{22}\Gamma_L|^2|1-\Gamma_{in}\Gamma_s|^2} \quad (6)$$

$$F_{min} = \left[1+2.4\left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega T}\right)\right] \quad (7)$$

$$G_A = \frac{P_{avl}}{P_A} = \frac{|S_{21}|^2\left(1-|\Gamma_s|^2\right)}{|1-S_{11}\Gamma_s|^2\left(1-|\Gamma_{out}|\right)^2} \quad (8)$$

where: $\Gamma_L=\Gamma_S=0$; $\Gamma_{in}=S_{11}$ and $\Gamma_{out}=S_{22}$.

The author has used an FR_4 substrate to design a low noise amplifier and has achieved perfect input-output matching, with good gain and minimum noise figure in 2.4 GHz frequency. In the article, it was mentioned that an additional series resistor at the transistor output increases stability, but there is no mention of the final stability factor. Power consumption is one of the important factors, yet no value indicates the power consumed by the LNA.

After careful study and observations, the conclusions were that common source is one of the topologies frequently used in the design of CMOS LNAs [27]. Inductive source degeneration gives high gain and low noise and is used in most circuits. When a transistor is used, the width and length of the transistor also account for the better performance of the LNA.

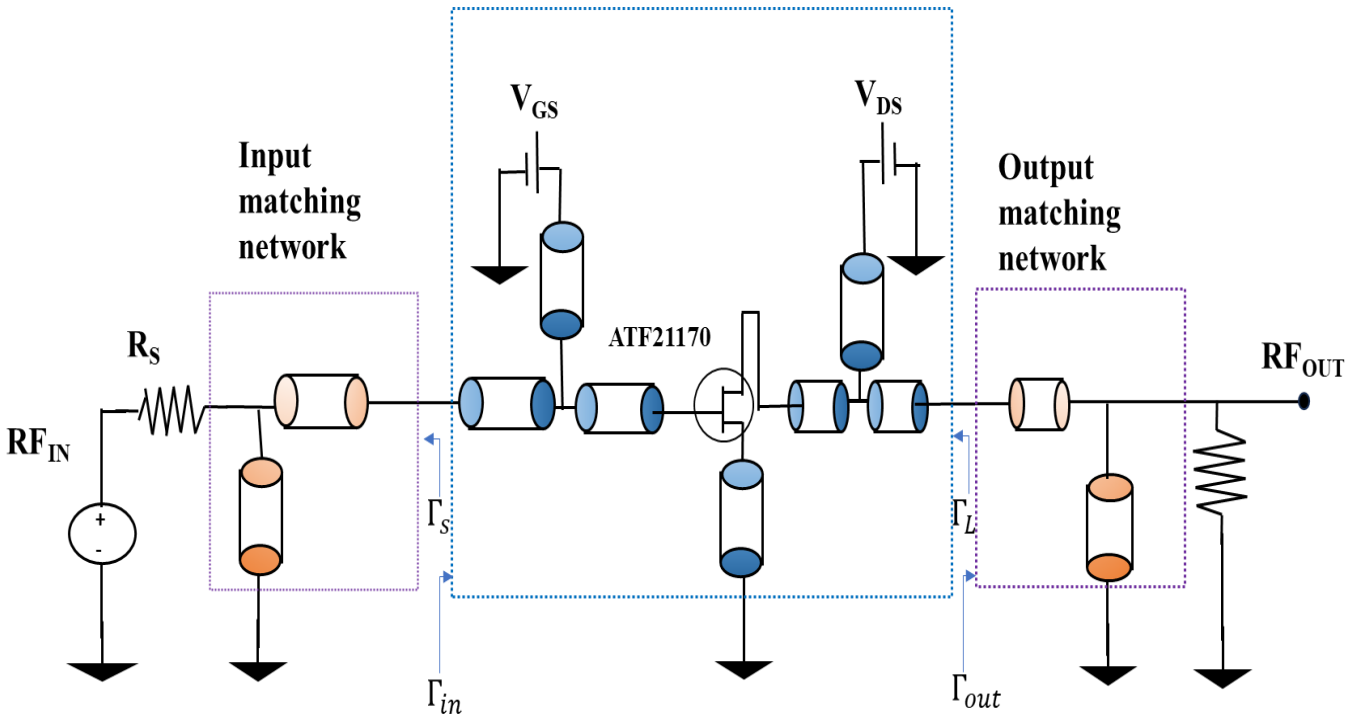

Fig. 6. LNA with cascode topology [26]

TABLE 1
COMPARISON OF DIFFERENT LNAS

Technology	Frequency (GHz)	S_{11} (dB)	S_{22} (dB)	Gain (S_{21}) (dB)	S_{12} (dB)	NF (dB)	Power consumption (mw)	V_{dd} (v)	Stability factor (k_f)	IIP3 point (dBm)	References
180 nm	2.4	-16.2	-11.06	24.89	-30.47	0.994	5.6	1.8	1.125	-6.16	[7]
NA	2.4	-10.02	-19.7	19.85	NA	1.014	NA	2	NA	NA	[18]
130 nm	2.4	10	12	12	NA	5.9	0.55	0.55	NA	-3	[19]
90 nm	2.4	NA	NA	28	NA	9.6	4.68	NA	NA	-12.8	[24]
NA	2.4	-70.35	72.98	30.69	NA	1.2	NA	NA	NA	NA	[25]
NA	2.4	-15.8	-15.8	15.11	NA	0.37	NA	NA	NA	14.8	[26]

Aside from the gain and noise figure, impedance matching is also a major factor contributing to the maximum power transfer at both ends. The circuits achieve a good impedance at input and output individually but when seen together for maximum power transfer, the obtained impedance matching is undesirable. The perfectly achieved impedance matching individually and combined has reasonable gain and a low noise figure [26].

In addition to RLCs, microstrip lines are used to design the LNA which gives better results for various parameters. The substrate used in the microstrip line must be chosen carefully, as with the values of the RLC components.

Based on an extensive literature review and thorough analysis of the findings presented in summary Table 1, the inductive degeneration topology was chosen as the preferred approach. Subsequently, the target specifications and objectives such as using 180 nm technology, with gain > 20 dB, and noise figure less than 2 dB at a frequency of 2.4 GHz were derived.

III. DESIGN APPROACH

The proposed LNA schematic, designed to achieve the desired gain at the resonant frequency of f_c = 2.4 GHz is illustrated in Fig. 8. The implementation of a CLC tank circuit at the input of the low-noise amplifier impacts its overall impedance matching and noise performance. The cascode topology of M_0 and M_1 used here provides excellent reverse isolation.

Transistor M_2 forms a current mirror with the M_1 transistor. The transistor sizes are determined using the g_m/I_d method, which aims to achieve maximum gain and a minimum noise figure without exceeding the consumption of power and the values are tabulated in Table II. The width of M_2 is (1/10) th of the width of M_1. To drive the transistors into region 2 of operation in Cadence (i.e., the saturation region), a current mirror biasing technique is used to provide the DC supply.

The inductor at the load minimizes noise, increasing the voltage swing in DC analysis. To isolate the output, a voltage-controlled voltage source (VCVS) with unity voltage gain can be inserted between the load and the output port (Port 1) [29-31]. The input port receives a sinusoidal signal at a frequency of 2.4 GHz.

TABLE 2
COMPONENT VALUES

Component	Value
C_1 & C_2	10 pF
C_0&C_3	50 pF
L_0	4.4 nH
L_1	200 pH
L_2	30 nH
$(W/L)_1$	80 u/ 180 n
$(W/L)_2$	80 u/ 180 n
$(W/L)_3$	8 u/ 180 n

It's worth noting that both the input and output ports maintain an internal resistance of 50 Ω, ensuring excellent input and output matching.

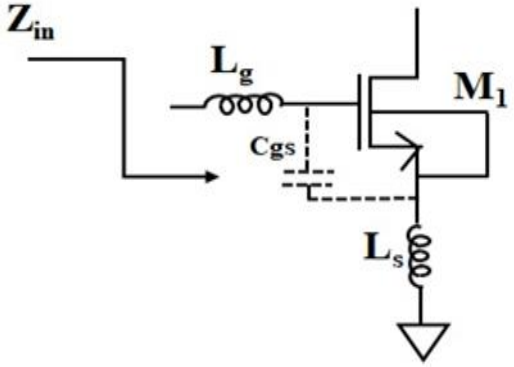

Fig. 7. Inductive source degeneration topology

For the sake of simplifying the analysis, let us consider a MOSFET model that comprises solely a transconductance and a gate-source capacitance as shown in Fig. 7. In such a scenario, the input impedance of the circuit, (Z_{in}) can be expressed as shown in Eq. (9)

$$Z_{in} = \frac{1}{sC_{gs1}} + s\left(L_s + L_g\right) + \frac{g_m L_s}{C_{gs1}} \qquad (9)$$

In the given equation, C_{gs1} represents the gate-to-source capacitance of M_1, L_s denotes the degeneration inductor, L_g

represents the gate inductor, and g_m represents the transconductance. The input impedance (Z_{in}) can be observed to consist of two components: a real part (Eq. (10)) that is frequency-independent and an imaginary part (Eq. (11)) that varies with frequency.

$$\frac{g_m L_s}{C_{gs1}} = 50\Omega \tag{10}$$

$$\frac{1}{sC_{gs1}} + s\left(L_s + L_g\right) = 0 \tag{11}$$

The operating power gain analyses can be done by Eqs. (12) & (13) [32]:

$$\text{Power gain (G)} = \frac{\text{Power delivered to the load}}{\text{power supplied to the amplifier}} \tag{12}$$

$$G = \frac{|S_{21}|^2\left(1-|\Gamma_L|^2\right)}{|1-S_{22}\Gamma_L|^2\left(1-|\Gamma_{in}|\right)^2} \tag{13}$$

Here the S_{21} is the gain
S_{22} is output reflection co-efficient.
Γ_L is load resistor and Γ_S is source resistor.
P_L is power delivered to the load
P_A is available power from the source
P_{in} is power supplied to the amplifier

In general, the gain and noise figure are the most considered in any amplifier circuit. The noise figure of an LNA is defined as the ratio of total noise power at the output to noise power at the output due to the input source. Hence recognizing the sources of noise is also a major task.

The resistors cause the thermal noise and the MOSFETs have the channel noise. Noise analyses for the proposed circuit can be done from the Eq. (7) [7]:

The Fig. 9 shows the layout of the proposed NB-LNA. As shown in the Fig. 9 the layout occupies a 1.25 mm of length and width of 0.833 mm.

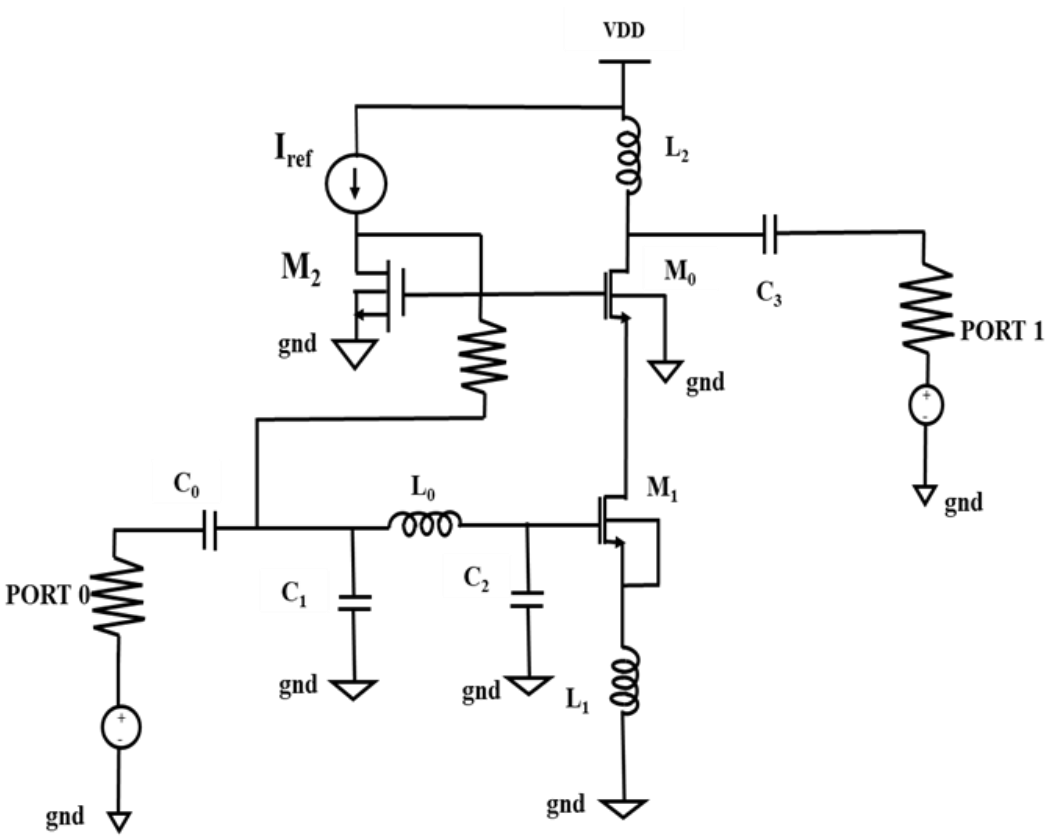

Fig. 8. Proposed current reused inductive degeneration common source low noise amplifier

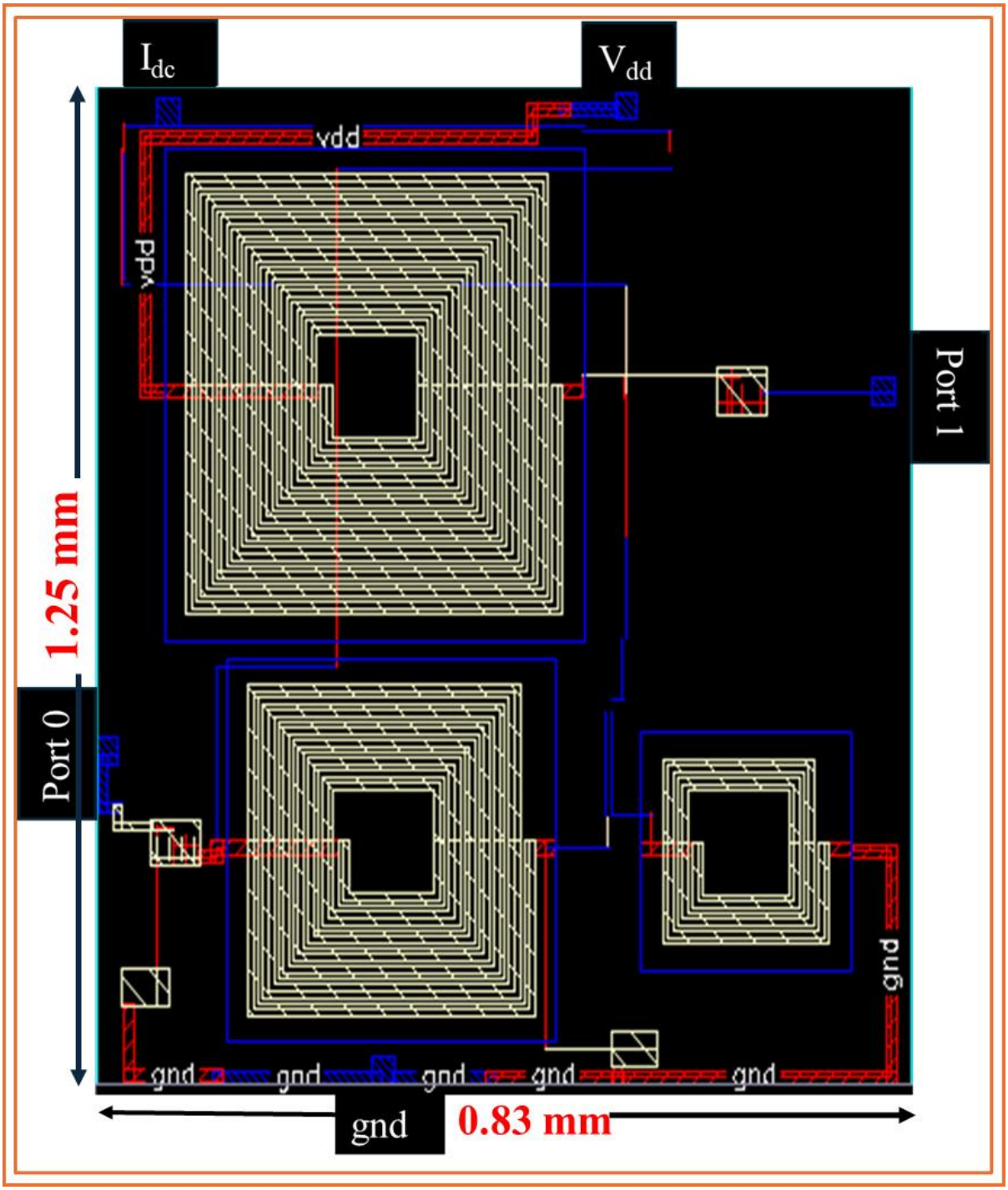

Fig. 9. The layout of the proposed low-noise amplifier

IV. RESULTS

The proposed LNA designed using Cadence Virtuoso with a supply voltage of 1.8 V and simulated using 180 nm technology consumed a power of 5 mW. Fig. 10 shows the S-parameters. Here the Input reflection co-efficient (S_{11}) in Fig. 10(a) is -17.17 dB, the reverse isolation (S_{12}) in Fig. 10(b) is -45.5 dB. The output reflection co-efficient (S_{22}) shown in Fig. 10(c) is -16.4 dB. The gain in Fig. 10(d) is 23.06 dB. Fig. 11 portraits noise figure and Fig. 12 displays stability factor.

For an LNA the important parameters to be considered are the S-parameters, noise measured in dB, and the stability factor (K_f) which are all represented in the above figures.

The performance of LNA is evaluated by different simulations wherein the process, voltage, and temperature are varied. The PVT analyses represent the sturdiness of the circuits under different conditions that exist after the fabrication [35, 36].

More precisely, the results conditions of PVT analysis typically involve the following aspects:

Process Variations: Assessing how discrepancies or

variations in the fabrication process—such as differences in doping concentrations, oxide thickness, or lithographic accuracy—affect the circuit's parameters, such as transistor characteristics, capacitances, resistances, and interconnects. The different processes are nominal-nominal corner (NN), fast-fast corner (FF), slow-slow corner (SS), slow-fast corner (SF), and fast-slow corner (FS).

Voltage Variations: Investigating the impact of variations in supply voltage levels on circuit behavior, including effects on power consumption, timing, noise margins, and functionality under different voltage conditions. Here the voltage is varied as 1.6 V, 1.8 V, and 2 V.

Temperature Variations: Analyzing the influence of temperature fluctuations on the performance of the IC, including effects on transistor threshold voltages, propagation delays, leakage currents, and overall reliability. Here the temperature is varied from -40°C, 27°C, and 80°C.

The goal of PVT analysis is to ensure that the designed circuit operates reliably and within specified performance limits under various process, voltage, and temperature conditions [37].

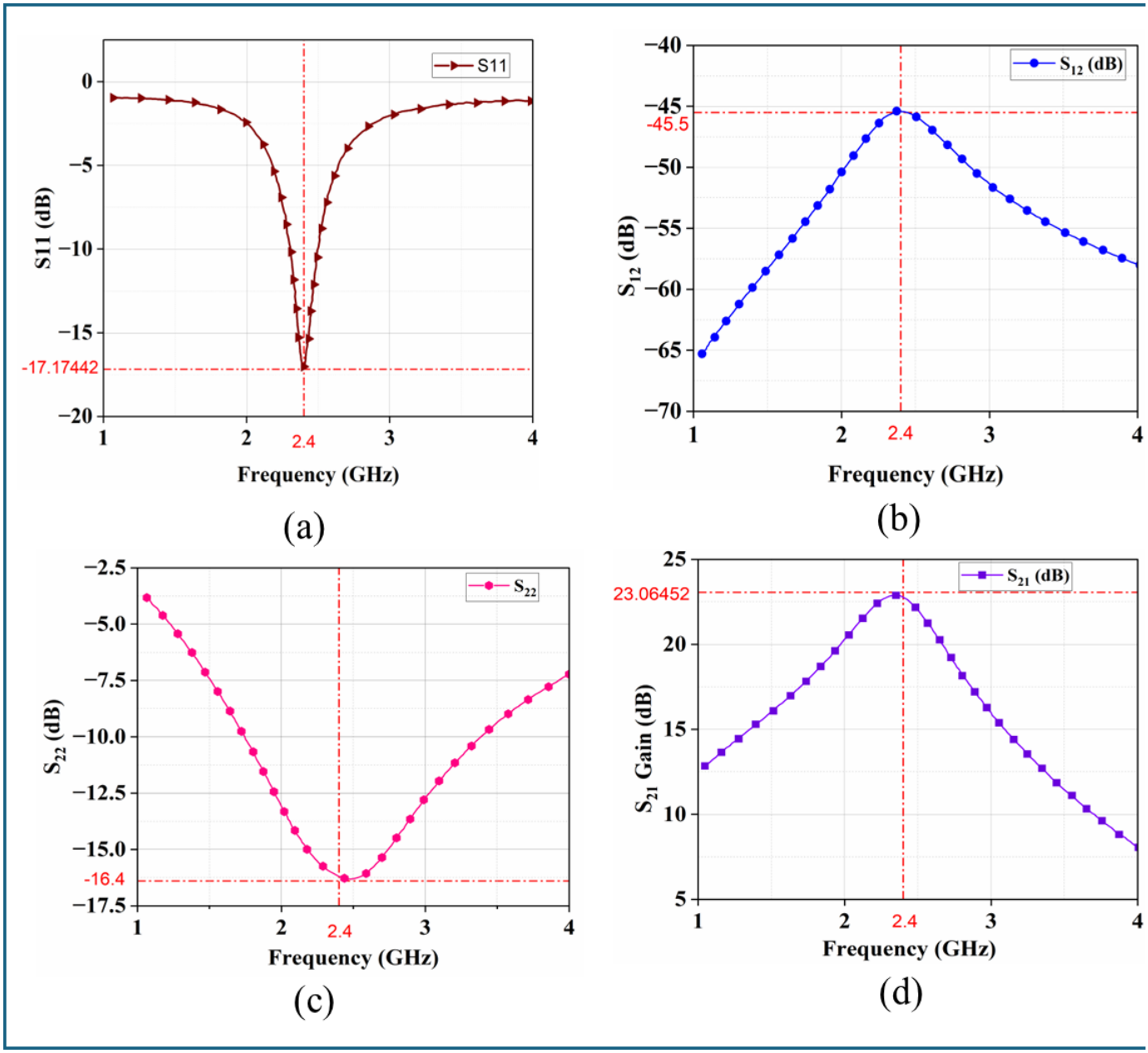

Fig. 10. Plot of S-parameters at 2.4 GHz

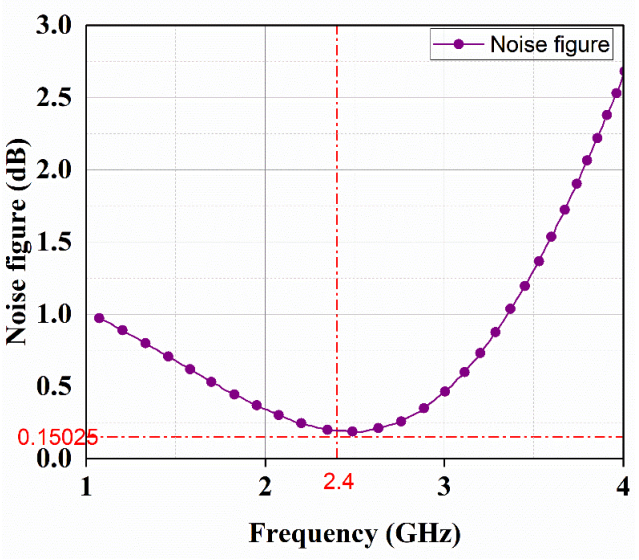

Fig. 11. Plot of noise figure at 2.4 GHz

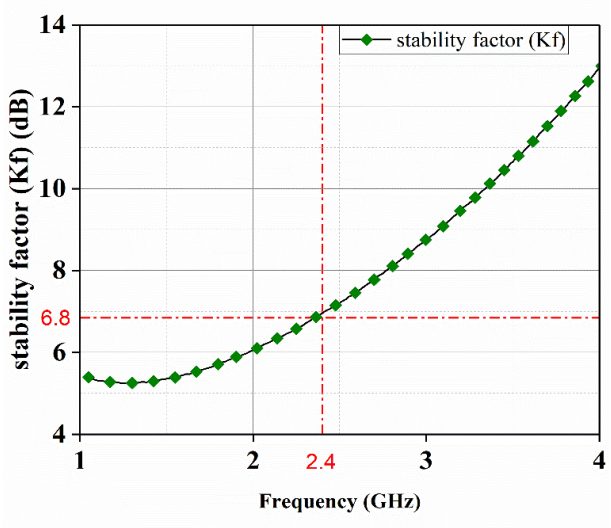

Fig. 12. Plot of stability factor at 2.4 GHz

The summary of PVT analyses as seen in Table III shows that the circuit's output parameters remain within the acceptable range and hence is stable and well-functioning irrespective of the changes in voltage, process, and temperature.

TABLE 3
SUMMARY OF PVT ANALYSES

Output	Minimum value (dB)	Mean value (dB)	Maximum value (dB)
S_{11}	-19.24	-9.36	-14.8
S_{12}	-52.04	-36.9	-44.47
S_{21}	17.56	26.24	21.9
S_{22}	-15.12	-16.48	-15.8
K_f	3.93	4.45	4.19

Deriving the observations from Table IV, it is noteworthy that our proposed circuit not only achieves a commendable balance between gain and noise performance but also excels in maintaining the crucial input and output impedance matching.

V. CONCLUSION

The constant development in wireless communication leads to increased research in low noise amplifiers specifically the narrow band LNAs. Applications such as RFID, Bluetooth, and Wi-Fi are major uses of narrowband LNA. In this article, narrow-band LNAs have been reviewed concerning circuit construction and advanced semiconductor technologies. Also, a single-stage inductive degenerated common source LNA with the current reuse technique has been presented with a 1.8 V supply.

The designed LNA not only achieved a good balance between gain and noise figures but also managed to have an input-output matching with a power consumption of 5 mW. The gain of the LNA is 23.06 dB, with a noise figure of 0.150 dB. The S_{11} is -17.17 dB and S_{22} is -16.4 dB. The reverse transmission co-efficient S_{12} is at -45.5 dB which denotes the least amount of signal transferred from the output port to the input port. The layout of the proposed schematic occupies a length of 1.2 mm with a width of 0.833 mm.

The stability factor of 6.8 shows that the circuit is unconditionally stable at the center frequency of 2.4 GHz. PVT analyses confirm the circuit's stability with variations in process, voltage, and temperature with minimal deviations from the targeted and typical values obtained.

TABLE 4
COMPARISON OF DIFFERENT LNAS

Technology	Frequency GHz	S_{11} (dB)	Gain (S_{21}) (dB)	S_{12} (dB)	S_{22} (dB)	Noise Figure (NF) (dB)	V_{dd} (V)	References
90 nm	2.4	-34	11	-42	-29	2.5	2.5	[26]
180 nm	2.4	-13.58	15.6	NA	-17.6	1.03	NA	[31]
90 nm	2.4	-1.826	25.17	-31.6	-2.17	1.3	1.2	[33]
90 nm	3.1-10.6	-10	12	NA	NA	1.6-2.1	1.5	[34]
180 nm	**2.4**	**-17.17**	**23.06**	**-45.5**	**-16.4**	**0.150**	**1.8**	**Present work**

ACKNOWLEDGMENTS

The authors are grateful to Vice Chancellor Dr. Indranil Manna of BIT Mesra for providing suitable lab and software. The authors are thankful to the editor and anonymous reviewers for the critical comments and constructive suggestions to improve the manuscript.

REFERENCES

[1] D. Sharma, A. Rai, S. Debbarma, O. Prakash, M K Ojha and V. Nath, "Design and Optimization of 4-Bit Array Multiplier with Adiabatic Logic Using 65 nm CMOS Technologies", *IETE Journal of Research*, pp. 1-14, 2023.

[2] D. Wu, R. Huang, W. Wong and Y. Wang, "A 0.4-V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application", *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 7, pp. 543-545, July 2007.

[3] S. P. Voinigescu et al., "A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1430-1439, Sept. 1997.

[4] D. J. Cassan and J. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 427-435, March 2003.

[5] S. Chehrazi, A. Mirzaei, R. Bagheri and A. A. Abidi, "A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-band use," *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference*, San Jose, CA, USA, 2005, pp. 801-804.

[6] R. Kundu, A. Pandey, S. Chakraborty, and V. Nath, "A CMOS Low Noise Amplifier based on Common Source Technique for ISM Band Application", *Microsystems Technologies*, vol. 22, pp. 2707-2714, 2016.

[7] D. Jahnavi, G. Kavya, and A. Jyothi Banu, "Design and Analysis of 2.4 GHz Low-Noise, High-Gain 0.18 μm CMOS Cascode Low-Noise Amplifier for IRNSS Applications," *IETE Journal of Research*, vol. 68, no. 6, pp. 3960–3970, 2020.

[8] A. Muthigi, A. Kumar, G. Bhagchandani, K. Muthigi, and V. Nath, "Automated Cheque Processing Through Data Verification and Siamese Networks, Microelectronics, Communication Systems", *Machine Learning and Internet of Things Lecture Notes in Electrical Engineering*, Springer, Singapore, 2023.

[9] A.Pandey, D. Kumar, R. Priyadarshi, and V. Nath, "Development of Smart Village for Better Lifestyle of Farmers by Crop and Health Monitoring System", *Microelectronics, Communication Systems, Machine Learning and Internet of Things*, Springer, vol. 887, Springer, Singapore, 2023.

[10] S. Kumar, Design of CMOS Low Noise Amplifier, *Microelectronics, Communication Systems, Machine Learning and Internet of Things, Lecture Notes in Electrical Engineering*, Springer, 2023

[11] K.K. Sharma, J.B. Sharma, and V. Nath, "Automatic Brain Tumor Detection and Segmentation from MRI Using Fractional Sobel Filter and SOM Neural Network, Microelectronics, Communication Systems", *Machine Learning and Internet of Things. Lecture Notes in Electrical Engineering*, Springer, pp. 441-454, 2023

[12] G. Sapone and G. Palmisano, "A 3–10-GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no.3, pp-678-686, 2011.

[13] W. Zhuo, "A capacitor cross-coupled common-gate low-noise amplifier", in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.59, pp.875-879, Dec. 2005.

[14] H. Zhang and E. Sánchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp.22-36, 2011.

[15] A. Ismail and A. A. Abidi, "A 3-10-GHz Low-Noise Amplifier with Wideband LC-ladder Matching Network", in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2269-2277, Dec. 2004.

[16] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 288-301, Jan. 2002.

[17] S. Ganesan, E. Sanchez-Sinencio and J. Silva-Martinez, "A Highly Linear Low-Noise Amplifier", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4079-4085, Dec. 2006.

[18] I.E Yilmaz, N.S. Tezel, "Low Noise Amplifier (LNA) Design Suitable for 2.4 GHz Radar Applications", in *Journal of Millimeter-wave Communication, Optimization and Modelling*, vol. 1, 2021.

[19] S. A. Zainol Murad, A. Azizan, R. Sapawi, and T.Z.A. Zulkifli, "Ultra-Low Power 0.55 mW 2.4 GHz CMOS Low-Noise Amplifier for Wireless Sensor Network", in *IETE Journal of Research*, vol. 68, pp. 2063–2068, 2019.

[20] H. -J. Liu and Z. -F. Zhang, "An Ultra-Low Power CMOS LNA for WPAN Applications", in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 174-176, Feb. 2017.

[21] M. Babasafari, and M. Yargholi, "A Low Power CMOS UWB LNA with Dual-band Notch Filter Using Forward Body Biasing", in *IETE Journal of Research*, vol. 66, no. 2, pp. 127–138, 2018.

[22] Z. Li, Z. Wang, M. Zhang, L. Chen, C. Wu, and Z. Wang, "A 2.4 GHz Ultra-low-power Current-reuse CG-LNA with Active GM-boosting Technique", in *IEEE Microwave and Wireless Components Letters*, vol. 24, pp. 348–350, 2014.

[23] A. F. Ahmad Fadhil Shuhaimi, N. H. Mohammad Amin, M. Muhamad, H. Hussin and J. Karim, "Gain Enhancement techniques of 0.13 μm CMOS Low Noise Amplifier", *IEEE Regional Symposium on Micro and Nanoelectronics (RSM), Kuala Lumpur, Malaysia*, 2021, pp. 165-168.

[24] R. Fiorelli, A. Villegas, E. Peralías, D. Vázquez and A. Rueda, "2.4-GHz Single-ended Input Low-power Low-voltage Active Front-end for ZigBee Applications in 90 nm CMOS", *20th European Conference on Circuit Theory and Design (ECCTD)*, Linköping, Sweden, 2011, pp. 829-832.

[25] B. Maruddani, M. Ma'sum, E. Sandi, Y. Taryana, T. Daniati, and W. Dara, "Design of two Stage Low Noise Amplifier at 2.4-2.5 GHz Frequency using Microstrip Line Matching Network Method", *Journal of Physics: Conference Series 044031*, vol. 1402, 2019.

[26] M. E. Bakkali, N. A. Touhami and T. Elhamadi, "Design at 2.4GHz Low Noise Amplifier for Wifi-Application", *2019 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS)*, Fez, Morocco, 2019, pp. 1-5.

[27] M.S. Kusuma, S. Shanthala, and C.Prasanna Raj, "Design of Common Source Low Noise Amplifier with Inductive Source Degeneration in Deep Submicron CMOS Processes", *International Journal of Applied Engineering Research*, vol. 13, pp. 4118-4123, 2018.

[28] J. Chaghaei, A. Jalali and M. Meghdadi, "Low-power Inductorless Current-reuse LNAs with Active and Passive G-enhancement", *Microelectron Journal*, vol. 97, pp. 104699, 2020.

[29] BM. Jafari and H. Shamsi, “A sub-1V Dual-path Noise and Distortion Canceling CMOS LNA for Low Power Wireless Applications”, in *Microelectron Journal*, vol. 104, pp. 104903, 2020.

[30] S. Jagarapu and R.K.Kavitha, “A 2.4 GHz Low Noise Amplifier in 0.18um CMOS Technology”, *IJCA Proceedings on International Conference on VLSI, Communications, and Instrumentation (ICVCI)*, vol. 10, pp. 10–15, 2011.

[31] A. Chopde, P. Sadar, A. Sabale, P. Thite, R.Zarkar, “Design of 2.4 GHz LNA of 400 MHz Bandwidth”, *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 11, pp. 65-69, 2022.

[32] R. Ludwig, and P. Bretchko, *RF Circuit Design: Theory and Applications*, Prentice Hall Press, 2000.

[33] D. Sam Chrisvin, M. Dharshini, S. N. Senthilkumar and T. Jaspar Vinitha Sundari, "Design and Study of 90nm CMOS Common Source 2.4GHz Low Noise Amplifier", *6th International Conference on Computing Methodologies and Communication (ICCMC)*, Erode, India, 2022, pp. 545-550.

[34] N. S. Amiri and M. Gholami, “Design of 3.1 to 10.6 GHz ultra-wideband flat gain LNA” *International Journal of Circuit Theory and Applications*, vol. 45, pp. 2034-2045, 2017.

[35] K A Mohamed Junaid, Y Sukhi , N Anjum et.al., “PV-based DC-DC Buck-boost Converter for LED Driver”, *Advances in Electrical Engineering, Electronics and Energy*, vol. 5, 2023.

[36] T. S Reddy, K.A. M Junaid, Y. Sukhi and Y. Jeyashree and P. Kavitha and V. Nath, “Analysis and Design of Wind Energy Conversion with Storage System”, *Advances in Electrical Engineering, Electronics and Energy*, vol. 5, 2023.

[37] P. Latha, V. Sumitra, T. Snehitha Reddy, Sunita Debbarma, Vijay Nath and V. Kannagi, “Optical Fiber Alignment Aid with Image Processing on FPGA-based System,” in *IETE Journal of Research*, 2023.